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10/051,397	01/17/2002	Scott B. Marovich	10003530-1	9611

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EXAMINER	
ISMAIL, SHAWKI SAIF	

ART UNIT	PAPER NUMBER
2155	

DATE MAILED: 04/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/051,397	MAROVICH, SCOTT B.	
	Examiner	Art Unit	
	Shawki S Ismail	2155	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *17 January 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-25 are presented for examination.

References in applicant's IDS form 1449 have been considered.

Claim Rejections - 35 USC §102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

3. Claims 1-25, are rejected under 35 U.S.C. 102(e) as being anticipated by **Gehman et al.,** (Gehman) U.S. Patent No. **6,304,553.**

4. As to claim 1, Gehman teaches a network interface for processing incoming messages sent by a client device to a server, comprising:

a First-In-First-Out (FIFO) buffer adapted to receive the incoming messages and to assemble the incoming messages from a serial to a parallel form (col. 1, lines 39-47, col. 4, lines 11-25); and

a regular-expression pattern matching circuit connected to the FIFO buffer, the regular-expression pattern matching circuit adapted to, concurrent with the assembly of the incoming messages from a serial to a parallel form, recognize Hypertext Transfer Protocol (HTTP) message headers embedded in the incoming messages, parse

recognized HTTP message headers into parsed HTTP message headers, and provide the parsed HTTP message headers to the server (col. 1, lines 13-24, col. 1, lines 39-47).

5. As to claim 2, Gehman teaches the network interface as claimed in claim 1 further including: a logic circuit connected to the FIFO buffer, the logic circuit adapted to provide a response message to the client device based on a content of the recognized HTTP message headers (col. 1, lines 55-63, col. 2, lines 43-55, col. 3, lines 12-15).

6. As to claim 3, Gehman teaches the network interface as claimed in claim 1 wherein: the regular-expression pattern matching circuit is further adapted to provide to the server the parsed HTTP message headers in a compact form (col. 1, lines 13-24, col. 1, lines 39-47).

7. As to claim 4, Gehman teaches the network interface as claimed in claim 1 wherein: the regular-expression pattern matching circuit is further adapted to provide to the server incoming messages that cannot be recognized by the regular-expression pattern matching circuit (col. 1, lines 13-24, col. 1, lines 39-47).

8. As to claim 5, Gehman teaches the network interface as claimed in claim 1 wherein: the regular-expression pattern matching circuit is implemented by a technique consisting of hardware, software, and a combination thereof (col.1, lines 39-48).

9. As to claim 6, Gehman teaches the network interface as claimed in claim 1 wherein: the HTTP message headers include HTTP cookies (col. 1, lines 13-24).

10. As to claim 7, Gehman teaches a network interface for processing incoming messages sent by a client device to a server, comprising:

a First-In-First-Out (FIFO) buffer adapted to receive the incoming messages and to assemble the incoming messages from a serial to a parallel form (col. 1, lines 39-47, col. 4, lines 11-25);

a regular-expression pattern matching circuit connected to the FIFO buffer, the regular-expression pattern matching circuit adapted to, concurrent with the assembly of the incoming messages from a serial to a parallel form, recognize Hypertext Transfer Protocol (HTTP) message headers embedded in the incoming messages, parse recognized HTTP message headers into parsed HTTP message headers, provide the parsed HTTP message headers in a compact form to the server, and provide to the server incoming messages that cannot be recognized by the regular-expression pattern matching circuit (col. 1, lines 13-24, col. 1, lines 39-47), wherein:

the HTTP message headers include HTTP cookies (col. 1, lines 13-24), and

the regular-expression pattern matching circuit is implemented by a technique consisting of hardware, software, and a combination thereof (col.1, lines 39-48); and

a logic circuit connected to the FIFO buffer, the logic circuit adapted to provide a response message to the client device based on a content of the recognized HTTP message header (col. 1, lines 55-63, col. 2, lines 43-55, col. 3, lines 12-15).

11. As to claim 8, Gehman teaches a server for providing services to a client device, comprising:

a central processing unit (CPU) (Fig. 1, col. 2, lines 43-55);

a bus connected to the CPU (Fig. 1, col. 2, lines 43-55);

a memory connected to the bus, the memory having a server application program stored therein (Fig. 1, col. 2, lines 43-55); and

a network interface for processing incoming messages sent by the client device to the server, the network interface including:

a First-In-First-Out (FIFO) buffer adapted to receive the incoming messages and to assemble the incoming messages from a serial to a parallel form (col. 1, lines 39-47, col. 4, lines 11-25), and

a regular-expression pattern matching circuit connected to the FIFO buffer, the regular-expression pattern matching circuit adapted to, concurrent with the assembly of the incoming messages from a serial to a parallel form, recognize Hypertext Transfer Protocol (HTTP) message headers embedded in the incoming messages, parse recognized HTTP message headers into parsed HTTP message headers, and provide the parsed HTTP message headers to the CPU and the memory, wherein the HTTP message headers include HTTP cookies (col. 1, lines 13-24, col. 1, lines 39-47, (col. 1, lines 13-24)).

12. As to claim 9, Gehman teaches the server as claimed in claim 8 further including: a logic circuit connected to the FIFO buffer, the logic circuit adapted to provide a response message to the client device based on a content of the recognized HTTP message headers (col. 1, lines 55-63, col. 2, lines 43-55, col. 3, lines 12-15).

13. As to claim 10, Gehman teaches the server as claimed in claim 8 wherein: the regular-expression pattern matching circuit is further adapted to provide to the CPU and

the memory the parsed HTTP message headers in a compact form (col. 1, lines 13-24, col. 1, lines 39-47).

14. As to claim 11, Gehman teaches the server as claimed in claim 8 wherein:

the regular-expression pattern matching circuit is further adapted to provide to the CPU and the memory incoming messages that cannot be recognized by the regular-expression pattern matching circuit (col. 1, lines 13-24, col. 1, lines 39-47).

15. As to claim 12, Gehman teaches the server as claimed in claim 8 wherein:

the HTTP message headers include HTTP cookies (col. 1, lines 13-24).

16. As to claim 13, Gehman teaches a server for providing services to a client device, comprising:

a central processing unit (CPU) (Fig. 1, col. 2, lines 43-55);

a bus connected to the CPU (Fig. 1, col. 2, lines 43-55);

a memory connected to the bus, the memory having a server application program stored therein (Fig. 1, col. 2, lines 43-55); and

a network interface for processing incoming messages sent by the client device to the server, the network interface including:

a First-In-First-Out (FIFO) buffer adapted to receive the incoming messages and to assemble the incoming messages from a serial to a parallel form (col. 1, lines 39-47, col. 4, lines 11-25),

a regular-expression pattern matching circuit connected to the FIFO buffer, the regular-expression pattern matching circuit adapted to, concurrent with the assembly of the incoming messages from a serial to a parallel form, recognize Hypertext Transfer

Protocol (HTTP) message headers embedded in the incoming messages, parse recognized HTTP message headers into parsed HTTP message headers, provide the parsed HTTP message headers in a compact form to the CPU and the memory, and provide to the CPU and the memory incoming messages that cannot be recognized by the regular-expression pattern matching circuit (col. 1, lines 13-24, col. 1, lines 39-47), wherein:

the HTTP message headers include HTTP cookies, and the regular-expression pattern matching circuit is implemented by a technique consisting of hardware, software, and a combination thereof (col.1, lines 39-48), and

a logic circuit connected to the FIFO buffer, the logic circuit adapted to provide a response message to the client device based on a content of the recognized HTTP message headers (col. 1, lines 55-63, col. 2, lines 43-55, col. 3, lines 12-15).

17. As to claim 14, Gehman teaches a communications network, comprising:

a client device (Fig. 1, col. 2, lines 43-55);

and a server connected to the client device for providing services to the client device (Fig. 1, col. 2, lines 43-55), the server including:

a central processing unit (CPU) (Fig. 1, col. 2, lines 43-55),

a bus connected to the CPU (Fig. 1, col. 2, lines 43-55),

a memory connected to the bus, the memory having a server application program stored therein, and a network interface for processing incoming messages sent by the client device to the server (Fig. 1, col. 2, lines 43-55), the network interface including:

a FIFO buffer adapted to receive the incoming messages and to assemble the incoming messages from a serial to a parallel form (col. 1, lines 39-47, col. 4, lines 11-25), and

a regular-expression pattern matching circuit connected to the FIFO buffer, the regular-expression pattern matching circuit adapted to, concurrent with the assembly of the incoming messages from a serial to a parallel form, recognize Hypertext Transfer Protocol (HTTP) message headers embedded in the incoming messages, parse recognized HTTP message headers into parsed HTTP message headers, and provide the parsed HTTP message headers to the CPU and the memory (col. 1, lines 13-24, col. 1, lines 39-47).

18. As to claim 15, Gehman teaches the communications network as claimed in claim 14 further including:

a logic circuit connected to the FIFO buffer, the logic circuit adapted to provide a response message to the client device based on a content of the recognized HTTP message headers (col. 1, lines 55-63, col. 2, lines 43-55, col. 3, lines 12-15).

19. As to claim 16, Gehman teaches the communications network as claimed in claim 14 wherein:

the regular-expression pattern matching circuit is further adapted to provide to the CPU and the memory the parsed HTTP message headers in a compact form (col. 1, lines 13-24, col. 1, lines 39-47).

20. As to claim 17, Gehman teaches the communications network as claimed in claim 14 wherein:

the regular-expression pattern matching circuit is further adapted to provide to the CPU and the memory incoming messages that cannot be recognized by the regular-expression pattern matching circuit (col. 1, lines 13-24, col. 1, lines 39-47).

21. As to claim 18, Gehman teaches the communications network as claimed in claim 14 wherein:

the HTTP message headers include HTTP cookies (col. 1, lines 13-24).

22. As to claim 19, Gehman teaches a communications network comprising:

a client device (Fig. 1, col. 2, lines 43-55); and

a server connected to the client device for providing services to the client device, the server including:

a central processing unit (CPU), a bus connected to the CPU (Fig. 1, col. 2, lines 43-55),

a memory connected to the bus, the memory having a server application program stored therein (Fig. 1, col. 2, lines 43-55), and

a network interface for processing incoming messages sent by the client device to the server, the network interface including:

a First-In-First-Out (FIFO) buffer adapted to receive the incoming messages and to assemble the incoming messages from a serial to a parallel form (col. 1, lines 39-47, col. 4, lines 11-25),

a regular-expression pattern matching circuit connected to the FIFO buffer, the regular-expression pattern matching circuit adapted to, concurrent with the assembly of the incoming messages from a serial to a parallel form, recognize Hypertext Transfer

Protocol (HTTP) message headers embedded in the incoming messages, parse recognized HTTP message headers into parsed HTTP message headers, provide the parsed HTTP message headers in a compact form to the CPU and the memory, and provide to the CPU and the memory incoming messages that cannot be recognized by the regular-expression pattern matching circuit (col. 1, lines 13-24, col. 1, lines 39-47), wherein:

the HTTP message headers include HTTP cookies (col. 1, lines 13-24), and

the regular-expression pattern matching circuit is implemented by a technique consisting of hardware, software, and a combination thereof (col.1, lines 39-48), and

a logic circuit connected to the FIFO buffer, the logic circuit adapted to provide a response message to the client device based on a content of the recognized HTTP message headers (col. 1, lines 55-63, col. 2, lines 43-55, col. 3, lines 12-15).

23. As to claim 20, Gehman teaches a method for processing incoming messages sent by a client device to a server, comprising:

receiving the incoming messages using a First-In-First-Out (FIFO) buffer;

assembling the incoming messages from a serial to a parallel form using the FIFO buffer (col. 1, lines 39-47, col. 4, lines 11-25); and

concurrent with the assembling of the incoming messages from a serial to a parallel form:

recognizing Hypertext Transfer Protocol (HTTP) message headers embedded in the incoming messages received by the FIFO buffer using a regular-expression pattern matching circuit (col. 1, lines 13-24, col. 1, lines 39-47),

parsing recognized HTTP message headers into parsed HTTP message headers using the regular-expression pattern matching circuit (col. 1, lines 13-24, col. 1, lines 39-47), and

providing the parsed HTTP message headers to the server (col. 1, lines 13-24, col. 1, lines 39-47).

24. As to claim 21, Gehman teaches the method as claimed in claim 20 further including:

providing a response message to the client device based on a content of the recognized HTTP message headers (col. 1, lines 13-24, col. 1, lines 39-47).

25. As to claim 22, Gehman teaches the method as claimed in claim 20 wherein:

the providing the parsed HTTP message headers to the server provides the parsed HTTP message headers in a compact form (col. 1, lines 13-24, col. 1, lines 39-47).

26. As to claim 23, Gehman teaches the method as claimed in claim 20 further including:

providing to the server incoming messages that cannot be recognized by the regular-expression pattern matching circuit (col. 1, lines 13-24, col. 1, lines 39-47).

27. As to claim 24, Gehman teaches the method as claimed in claim 20 wherein:

the HTTP message headers include HTTP cookies (col. 1, lines 13-24).

28. As to claim 25, Gehman a teaches the method for processing incoming messages sent by a client device to a server, comprising:

receiving the incoming messages using a First-In-First-Out (FIFO) buffer (col. 1, lines 39-47, col. 4, lines 11-25);

assembling the incoming messages from a serial to a parallel form using the FIFO buffer (col. 1, lines 39-47, col. 4, lines 11-25);

concurrent with the assembling of the incoming messages from a serial to a parallel form (col. 1, lines 13-24, col. 1, lines 39-47),

recognizing Hypertext Transfer Protocol (HTTP) message headers embedded in the incoming messages received by the FIFO buffer using a regular-expression pattern matching circuit (col. 1, lines 13-24, col. 1, lines 39-47),

parsing recognized HTTP message headers into parsed HTTP message headers using the regular-expression pattern matching circuit, and providing the parsed HTTP message headers to the server in a compact form; providing a response message to the client device based on a content of the recognized HTTP message headers (col. 1, lines 13-24, col. 1, lines 39-47); and

providing to the server incoming messages that cannot be recognized by the regular-expression pattern matching circuit (col. 1, lines 13-24, col. 1, lines 39-47).

Conclusion

29. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shawki S Ismail whose telephone number is 571-272-3985. The examiner can normally be reached on M-F 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hosain Alam can be reached on 571-272-3978. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Shawki Ismail
Patent Examiner
March 29, 2005

HOSAIN ALAM
SUPERVISORY PATENT EXAMINER